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EXAMINER	
MAI, ANH D	

ART UNIT	PAPER NUMBER
2814	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/254,939	MIURA ET AL.	
	Examin r	Art Unit	
	Anh D. Mai	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 March 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-6,9,10,12,13,15,18-39 and 41-66* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,9,10,12,13,15,18-39 and 41-66* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Status of the Claims

1. Amendment filed March 23, 2004 has been entered. Claims 3, 9, 12, 13, 46 and 54 have been amended. Claims 56-66 have been added. Claims 1-6, 9, 10, 12, 13, 15, 18-39 and 41-66 are pending.

Response to Amendment

2. The amendment filed March 23, 2004 is objected to under 35 U.S.C. 132 because it introduces new matter into the disclosure. 35 U.S.C. 132 states that no amendment shall introduce new matter into the disclosure of the invention. The added material which is not supported by the original disclosure is as follows: "wherein said chemically mechanically polished surface is formed over said circuit formation surface and over said trench, and wherein in performing the selective thermal oxidation, said semiconductor substrate having said chemically mechanically polished surface formed over said circuit formation region and over said trench is selectively thermally oxidized" (claims 55-66).

Applicant is required to cancel the new matter in the reply to this Office Action.

Claim Rejections - 35 USC § 112

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

3. Claims 55-66 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not

described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention.

There does not appear to be a written description of the claim limitation "wherein said chemically mechanically polished surface is formed over said circuit formation surface and over said trench, and wherein in performing the selective thermal oxidation, said semiconductor substrate having said chemically mechanically polished surface formed over said circuit formation region and over said trench is selectively thermally oxidized" in the application as filed.

Claim Objections

4. Claims 64 and 65 are objected to because of the following informalities: both claims depend on claim 45 and recite the same limitation.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

5. Claims **1**, **9**, **10**, 12, 13, **15**, 18-20, 30-39, **41**, 42, 46-49 and 52 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta et al. (U.S. Patent No. 5,646,063) of record.

With respect to claim **1**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate (14); (Fig. 4);

(c) thermally oxidizing a trench portion formed in the semiconductor substrate (14), exposed in the trench (44) so as to form a first curvature of the upper end portion of the trench (44); (Fig. 5);

(d) burying a buried insulating film (60) into the trench (44) so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18); (Fig. 5);

(e) after burying the buried insulating film (60), removing the insulating film (60) on the oxidation prevention film (18), by chemical mechanical polishing (CMP), thereby forming a chemically mechanically polished surface (66); (Fig. 6);

(f) after the removing, performing selective thermal oxidation of the semiconductor substrate (14) after having formed the CMP polished surface (66), so as to thermally oxidize only a portion of the semiconductor substrate (14) at the upper end portion of the trench (44), and not substantially at other portion of the semiconductor substrate lining the trench (44), so as to increase a curvature of the upper end portion of the trench (44) substantially without oxidizing the other portions of the semiconductor substrate lining the trench (44); (Fig. 9);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

With respect to the limitation "thermally oxidizing", the term "thermally grown" of Mehta (col. 5, ll. 30-35) is recognized in the art as thermally oxidizing. The thermal oxidation that form liner oxide (56) of Mehta is well known in the art to generate a bird's beak at the interface of the oxidation prevention film (18) and the upper corner of trench (44), thus, first curvature.

The "chemical mechanical planarization" of Mehta '063 is also known as chemical-mechanical polishing.

With respect to "selective thermal oxidation" of step (f), since Mehta only oxidize the upper corner of the oxide in the trench, thus, the limitation of the claim is met.

With respect to claim **9**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming trench regions (44) in the substrate from the circuit formation surface thereof;

(c) performing a first thermal oxidation to form an oxide film (56) on the trench regions (44) formed in step (b), and to form a first curvature at upper end portions of trench regions (44) formed in step (b), and

(d) forming an insulating film (60) inside the thermally oxidized trench regions (44) so as to completely fill them, thereby forming completely filled trench regions, and forming the insulating film (60) on the oxidation prevention film (18),

(e) removing the insulating film (60) formed on the oxidation prevention film (18) by chemical mechanical polishing (CMP), thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing a selective thermal oxidation, of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), so as to selectively oxidize only an opening side of the completely filled trench regions (44) in the substrate (14), and not substantially at other portions of the semiconductor substrate lining trench regions (44), substantially without oxidizing the other portions of the semiconductor substrate lining trench regions (44); and

(g) after performing the selective thermal oxidation, removing the oxidation prevention film (18), and forming a gate oxide film (135). (See Figs. 1-9).

With respect to "thermally oxidizing" ; "chemical mechanical planarization" and "selective thermal oxidation", the similar reasoning as that of claim 1 also apply.

With respect to claim **10**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate, the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate (14);

(c) thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench (44) so as to form a first curvature at upper end portion of trench (44);

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18) by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after removing, performing selective thermal oxidation of the semiconductor substrate (14), after having formed the chemically mechanically polished surface, so as to oxidize only apportion of the semiconductor substrate, at the upper end portion of the trench and not substantially at other portions of the semiconductor substrate lining the trench (44), to increase the curvature of the upper end portion of trench (44), substantially without oxidizing the other portions of the semiconductor substrate lining the trench (44); and

(g) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14). (See Figs. 1-9).

With respect to "thermally oxidizing" ; "chemical mechanical planarization" and "selective thermal oxidation" the similar reasoning as that of claim 1 also apply.

With respect to claim 12, the increased curvature of Mehta includes forming a well known bird's beak at the upper end portion of the trench. (see Fig. 1).

With respect to claim 13, the increased curvature of Mehta is formed such that an angle (θ) between the circuit formation surface of the semiconductor substrate (14) and a side surface of the semiconductor substrate forming the trench is within a range of $90° < \theta < 180°$.

With respect to claims 49 and 52, the oxidation prevention film (18) of Mehta is eliminated or removed after thermally oxidizing only a portion of the semiconductor substrate.

With respect to claim **15**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion thereof extending to the circuit formation surface of the semiconductor substrate;

(c) thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in trench (44), so as to provide the upper end portion of the trench (44) with a curvature;

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), having the buried insulating film (60) in trench (44), by CMP thereby forming a chemically mechanically polished surface (66);

(f) after removing, performing selective thermal oxidation of semiconductor substrate (14), after having formed the chemically mechanically polished surface (66) only at the upper

portion end portion of trench (44), to increase the curvature of the upper end portion of trench (44) as compared with the curvature provided in step (c), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44); and

(g) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14). (See Figs. 1-9).

With respect to "thermally oxidizing" ; "chemical mechanical planarization" and "selective thermal oxidation" the similar reasoning as that of claim 1 also apply.

With respect to claims 18-20 and 30-38, the buried insulating film of Mehta is silicon oxide, deposited by CVD.

With respect to claim 39, the step (f) of removing the oxidation prevention film (18) of Mehta is performed after the performing thermal oxidation.

With respect to claim **41**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate;

(c) thermally oxidizing a trench portion formed in the semiconductor substrate (14), exposed in trench (44), forming a curvature of the upper end portion of trench (44);

(d) burying a buried insulating film (60) into trench (44) so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing selective thermal oxidation of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), only at the upper end portion so as to provide an increased curvature of the upper end portion of trench (44) as compared with the curvature formed in step (c), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after the eliminating, forming a gate oxide film (135). (See Figs. 1-9).

With respect to "thermally oxidizing" ; "chemical mechanical planarization" and "selective thermal oxidation" the similar reasoning as that of claim 1 also apply.

With respect to claim 42, step (g) of eliminating the oxidation prevention film (18) is performed after step (f) of selectively thermally oxidizing the semiconductor substrate (14) at the upper end portion.

With respect to claim **46**, Mehta '063 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench regions (44) in the substrate from the circuit formation surface thereof;

(c) performing a first thermal oxidation to form an oxide film (56) on trench regions (44) formed in step (b), so as to provide a curvature at an opening side of trench regions (44); and

(d) forming an insulating film (60) inside the thermally oxidized trench regions (44) so as to completely fill them, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing a selective thermal oxidation of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66) to selectively oxidize only the opening side of the completely filled trench regions (44) in substrate (14) so as to provide an increased curvature at the opening side as compared to the curvature provided in step (c), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44); and

(g) after performing the selective oxidation, removing the oxidation prevention film (18) and forming a gate oxide film (135). (See Figs. 1-9).

With respect to "thermally oxidizing" ; "chemical mechanical planarization" and "selective thermal oxidation" the similar reasoning as that of claim 1 also apply.

With respect to claim **47**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined positions of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portions thereof extending to the circuit formation surface of the semiconductor substrate (14);

(c) thermally oxidizing a trench portions formed in semiconductor substrate (14), exposed in the trenches (44), there by providing the upper end portion of the trench with a radius curvature;

(d) burying a buried insulating film (60) into the trench (44) so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, providing the upper end portion of the trench (44) with an increased radius of curvature, as compared with the radius of curvature provided in step (c), by performing selective thermal oxidation only of the upper end portion of trench (44) of the semiconductor substrate (14) after having formed the chemically mechanically polished surface

(66), substantially without oxidizing other portions of the semiconductor substrate (14) lining trench (44); and

(g) removing the oxidation film prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14). (See Figs. 1-9).

With respect to "thermally oxidizing" ; "chemical mechanical planarization" and "selective thermal oxidation" the similar reasoning as that of claim 1 also apply.

With respect to claim 48, step (g) of eliminating or removing the oxidation prevention film (18) is performed after step (f) of selectively thermally oxidizing the semiconductor substrate (14) at the upper end portion or providing the upper end portion of the trench (44) with an increased radius of curvature.

6. Claims 56, 60-63 and 66 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '063 as applied to claims 1, 9, 10, 15, 41 and 47 above, and further in view of Otsu (U.S. Patent No. 5,236,861) of record.

With respect to claims 56, 60-63 and 66Mehta is shown to teach all the features of the claim with the exception of performing the selective thermal oxidation on the CMP surface of the buried insulating film to increase the curvature.

However, Otsu teaches to increase the curvature (a) of the upper corner of the trench, a selective thermal oxidation is performed on the CMP surface of the buried insulating film (9). (See Fig. 3E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to increase the curvature at the upper corner of trench (44) of Mehta by performing selective thermal oxidation on the CMP surface of the buried insulating film as taught by Otsu to reduce leakage current.

7. Claims **2**-6, 21-29, **43**-45 and 53-55 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '063 in view of Takahashi (EU. Patent No. 0459397) of record.

With respect to claims **2** and **43**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(c) forming trenches (44) having a predetermined depth in semiconductor substrate (14);

(d) thermally oxidizing trench portions formed in the semiconductor substrate (14), exposed in the trenches (44), so as to form a radius curvature at the corners, at upper end portion of trenches (44);

(e) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(f) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(g) after the removing, performing selective thermal oxidation of semiconductor substrate (14), so as to oxidize only a portion of semiconductor substrate (14) extending from the corners, and not substantially at other portions of the semiconductor substrate lining trenches (44), so as

to increase the radius of curvature of trenches (44), substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(h) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(i) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Thus, Mehta is shown to teach all the features of the claim with the exception of forming the trenches (44) using two steps etching.

However, Takahashi '397 teaches forming a trench using two steps etch including:

(b) forming shallow trenches (26) having a radius curvature (27) at the corners in a desired position of the circuit formation surface of a semiconductor substrate (22); (Fig. 2B);

(c) forming trench (28) having a predetermined depth to the shallow trenches (26) having a radius of curvature (27) so formed. (See Figs. 2A-C).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to form the trenches of Mehta using two steps etching as taught by Takahashi to reduced leakage current.

With respect to claims **4** and **45**, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming trench having a predetermined depth at a desired positions of the circuit formation surface of semiconductor substrate (14), the trench having an upper end portion;

(c) thermally oxidizing trench portions formed in semiconductor substrate (14), exposed in the trench, so as to forms a first curvature of the upper end portions of trenches (44);

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film(60) also being formed on the oxidation prevention film (18);

(e) removing the insulating film (60) on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(f) after the removing, performing selective thermal oxidation of semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), so as to oxidize only a portion of semiconductor substrate at the upper end portion of trenches (44), and not substantially at other portions of the semiconductor substrate lining trenches (44), the upper end portions being oxidized, so as to increase a curvature of the upper end portions of trenches (44), substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(g) removing the oxidation preventing film (18) formed on the circuit formation surface of the semiconductor substrate (14); and

(h) after the oxidizing the semiconductor substrate, forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of trenches having upper end portions not covered by the oxidation prevention film, the similar reasoning as that of claims **2** and **43** is also applied here. Note that, forming trenches by two step etching of Takahashi is result in trench (28) having upper end portion (27) not covered by the oxidation prevention film (23). (See Fig. 2C).

With respect to claim **5**, as best understood by the examiner, Mehta teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(c) forming trenches (44) having a predetermined depth in semiconductor substrate (14);

(d) thermally oxidizing trench portions formed in the semiconductor substrate (14), exposed in the trenches (44), so as to form a radius of curvature of the corner, at upper end portions of trench (44);

(e) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(f) removing the insulating film (60) formed on the oxidation prevention film (18), by CMP, thereby forming a chemically mechanically polished surface (66);

(g) after the removing, performing selective thermal oxidation of the semiconductor substrate (14) after having formed the chemically mechanically polished surface (66), so as to oxidize only a portion of the semiconductor substrate extending from the corners, and not substantially at other portions of the semiconductor substrate lining trenches (44), so as to increase the radius of curvature of the trenches corner, substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(h) removing the oxidation prevention film (18) formed on the circuit formation surface of the semiconductor substrate (14); and

(i) after the thermally oxidizing the semiconductor substrate (14), forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of shallow trenches having radius of curvature, the similar reasoning as that of claims **2** and **43** also apply.

With respect to claims 3, 6, the step for forming shallow trenches (26) of Takahashi is carried out by isotropic etching and the step of forming trenches (28) is carried out by anisotropic etching to a predetermined depth.

With respect to claims 21-29, the buried insulating film (60) of Mehta is silicon oxide, deposited by CVD.

With respect to claim 44, step (h) of Mehta is performed after step (g).

With respect to claim 51, the oxidation prevention film (18) of Mehta '063 is removed after the oxidizing only portion of the semiconductor substrate.

With respect to claims 50 and 53, the oxidation prevention film (120) of Mehta '599 is removed after the oxidizing only portion of the semiconductor substrate.

With respect to claim **54**, Mehta '063 teaches a method of fabricating a semiconductor device substantially as claimed including:

(a) forming an oxidation prevention film (18) on a circuit formation surface of a semiconductor substrate (14);

(b) forming a trench (44) having a desired depth at a predetermined position of the circuit formation surface of the semiconductor substrate (14), the trench having an upper end portion adjacent the circuit formation surface of the semiconductor substrate (14), trench (44) being formed by anisotropic etching the semiconductor substrate (14);

(c) thermally oxidizing the trench portions formed in the semiconductor substrate (14), exposed in the trenches (44);

(d) burying a buried insulating film (60) into the trench so thermally oxidized, the insulating film (60) also being formed on the oxidation prevention film (18);

(e) after burying the buried insulating film(60), performing an additional selective thermal oxidation so as to selectively oxidize the semiconductor substrate at the upper end portion of the trench (44), to increase the radius of curvature in the proximity of the upper end portion of trench (44), and substantially without oxidizing other portions of the semiconductor substrate lining trench (44);

(f) after burying the buried insulating film (60), removing the insulating film (60) on the oxidation prevention film (18);

(g) eliminating the oxidation prevention film (18) formed on the semiconductor substrate; and

(h) after eliminating, forming a gate oxide film (135). (See Figs. 1-9).

Regarding the formation of trench using two steps etching, the similar reasoning as that of claims **2** and **43** also apply.

Note that, trench (28) of Takahashi is formed by first etch using isotropic etching to form trench (26), so as to form a radius of curvature in the proximity of the upper end portion, and by the second etch using anisotropic etching to form trench (28). (See Figs. 2A-C).

With respect to claim 55, performing an additional thermal oxidation of Mehta is performed after removing the insulating film (60) on the oxidation prevention film (18).

8. Claims 57-59, 64 and 65 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mehta '063 and Takahashi '397 as applied to claims 2, 4, 5 and 45 above, and further in view of Otsu (U.S. Patent No. 5,236,861) of record.

With respect to claims 57-59, 64 and 65, Mehta and Takahashi are shown to teach all the features of the claim with the exception of performing the selective thermal oxidation on the CMP surface of the buried insulating film to increase the curvature.

However, Otsu teaches to increase the curvature (a) of the upper corner of the trench, a selective thermal oxidation is performed on the CMP surface of the buried insulating film (9). (See Fig. 3E).

Therefore, it would have been obvious to one having ordinary skill in the art at the time of invention to increase the curvature at the upper corner of trench (44) of Mehta by performing selective thermal oxidation on the CMP surface of the buried insulating film as taught by Otsu to reduce leakage current.

Response to Arguments

9. Applicant's arguments filed March 23, 2004 have been fully considered but they are not persuasive.

With respect to new matters: (claims 55-66)

Applicants insist that new claims as well as previously cancelled claims do not contain new matters.

However, as discussed in the previous Office Action, as well as the present, Applicants fail to point out the specific portion of the original written disclosure directed to such matters, e.g., additional oxidation is performed on the CMP surface.

Page 8, line 3-5, specifically states: this step (additional oxidation) may be executed **before** the step (6) (before CMP) or **after** the next step (8) (after remove the oxidation prevention and pad oxide).

Page 23, line 12-19, states: "When the radius of curvature of the trench upper end portion due to the bird's beak grown by the oxidation of the trench portion of the silicon substrate is not sufficient for preventing the increase of the leakage current, thermal oxidation is again carried out (hereinafter called "additional oxidation") **before the buried insulating film 9 is etched back** (Fig. 6L, Fig. 7 (312)".

Insofar as 6K is concerned, Fig. 6K is the result of CMP on the oxide 9 of Fig. 6G, when the curvature is sufficient to prevent leakage current, then additional oxidation is not necessary.

Also in Fig. 7, the additional oxidation (311) is performed before the etchback (CMP) (312).

New claims 55-66 contain new matters, removal of these new matters are required.

With respect to Art rejection:

Applicants argue that the applied references have neither taught not would have suggest such a method as in the amended claims including: after forming a trench or trench region, thermally oxidizing a trench portion formed in the semiconductor substrate, exposed in the trench, so as to form, e.g., a first curvature of the upper end portions of the trench, and after burying a buried insulating film into the trench and on an oxidation prevention film on a substrate having the trench formed therein, removing the insulating film by chemical mechanical polishing and thereafter performing selective or additional thermal oxidation of the substrate after having formed the chemically mechanically polished surface, so as to thermally oxidize only a portion of the substrate, at the upper end portion of the trench, and not substantially at other portions of the substrate lining the trench, so as to increase a curvature of the upper end portion of the trench substantially without oxidizing the other portions of the semiconductor substrate lining the trench.

Applicants appear to reproduce the same argument presented previously without specifically identify elements of the claims which allegedly, do not teach by the references. Therefore, the same response is applied.

All of these element are clearly taught by Mehta. (See rejection above).

1) with respect to "thermally oxidizing a trench portion", the liner oxide 56 is formed by **thermally grown**, hence, thermally oxidizing. One having ordinary skill in the art would have known this. The formation of "curvature of the upper end portion" or rounding of the corner by

forming thermal liner are well documented. Applicants are urged to sturdy C.P Chang et al. (PTO 892, paper # 14).

2) with respect to "after burying a buried insulating film into the trench and on an oxidation prevention film on a substrate having the trench formed therein, removing the insulating film by chemical mechanical polishing", see Mehta's Fig. 6. Applicants appear to not fully understand that chemical mechanical planarization is the same as chemical mechanical polishing.

3) with respect to "and thereafter performing selective or additional thermal oxidation of the substrate after having formed the chemically mechanically polished surface", Mehta teaches "After layer 60 is subjected to an oxide etch, structure 12 is subjected to thermal oxidation to grow the oxide in spacing 44" (see col. 5, ll. 54-56). Note that, the thermal oxidation is performed after the chemically mechanically polished surface 66 have been formed, thus, encompasses the claimed. Also note that, the additional thermal oxidation of Mehta only oxidize the upper end portion of trench (44) thus, forming the bird's beak, thus, increase the curvature (formed by thermal liner) of the upper end portion and the rest of trench (44) still remained. (See Fig. 9).

Applicants also added: and in fact would have taught away from, the method. It appears that that the Applicants fails to identify which portions that taught away from the invention as claimed.

With respect to two steps etching, Takahashi clearly teaches that.

The remaining arguments only a repetition of the previous argument, thus, the same response is applied.

Conclusion

10. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Anh D. Mai whose telephone number is (571) 272-1710. The examiner can normally be reached on 9:00AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Wael Fahmy can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

A.M
May 27, 2004

Wael Fahmy
SPE 2814